REMARKS/ARGUMENTS:

Claims 1-21 are pending in this application. In the Office Action dated December 15, 2006, the Examiner has made the following conclusions:

- Claims 4-6 rejected under 35 USC 112, first paragraph for failing to define the claim 4 term "error-formatter" in the written description;
- Claims 4-5 are objected for lacking antecedent basis for the term "fractional interpolator filter";
- Claims 1-7, 10-11, and 13-19 are rejected under 35 USC 103(a) as obvious over Mueller (US Pub 2003/0204542) in view of Gardner (US 5,805,619);
- Claims 2-3 and 12 are rejected under 35 USC 103(a) as obvious over Mueller, Gardner and Boerstler (US 6,353,369);
- Claims 20-21 are rejected under 35 USC 103(a) as obvious over Mueller, and Harnden (US Pub. 2003/0069009); and
- Claims 8-9 are objected as depending from a rejected base claim but otherwise would be allowable if rewritten in independent form.

These are addressed in order below. Claim 4 is amended to replace "error formatter" with "bit splitter", shown at Fig. 5 (ref 68) and page 9 lines 24-25, as well as Fig. 4 (shown as the "MSB" split from output A-4 of the delay register 60). Claim 4 is also amended in its preamble to delete "filter" from "fractional interpolator filter".

For the obviousness rejections over only Mueller and Gardner, claims 1, 17 and 18 are directed to a circuit, and claim 13 is directed to a method.

It is known to use fractional re-sampling in multi-rate systems. When used in a demodulator (the receive end of a communication, as opposed to a modulator at the transmit end of the communication), use of digital timing error correction has also been introduced as part of digital modems. This timing error correction refers to symbol timing synchronization that must be implemented as part of the demodulator. Mueller concerns fractional interpolation at the modulator. Gardner (the inventor, not necessarily the cited reference) is recognized as a key researcher in the field of fractional interpolation at the demodulator. The Examiner relies upon Gardner's timing error detector 106 at the demodulator as relevant to the timing error detector sub-circuit of claim 1 and the detector loop of claim 18.

As seen in Figure 2, embodiments of this invention are detailed with respect to the transmit side of a communication, the modulator. In both this invention and Mueller, fractional re-sampling is implemented at the modulator by decoupling the symbol-rate clock from the digital-to-analog converter (DAC) sampling clock. This can be thought of as asynchronous sampling since the symbol-rate clock and the DAC sample-rate clock are not related by an integer factor, though in truth these clocks must be synchronized by some digital means. Generically term this some kind of a digital symbol-rate (and data-rate) synchronization circuit. This allows crossing the boundary from the symbol-rate clock domain to the sample-rate clock domain. It is this boundary crossing that is fundamentally different as between the modulator and the demodulator side of a communication, and the clearest distinction over Gardner and Harnden. Those two references address symbol timing recovery and phase recovery at the demodulator, and address the problem of fractional interpolation at the demodulator/receiver by synchronizing the receiver *to the transmitter* – synchronization of symbol timing clocks as noted above. In claim 1, the symbol rate clock is synchronized to the oscillator (sample rate clock) via the strobe (claim 1 recites a timing error detector sub-circuit that has a strobe input from the oscillator and also an input from the symbol rate clock, and the oscillator has an input from the timing error detector sub-circuit). Claim 1 is amended to recite that the oscillator is a numerically controlled oscillator to more clearly distinguish the terminology over Gardner, over and above the difference in timing signals that are synchronized to one another as noted above. Because Gardner does not operate with timing signals analogous to those used within the modulator teachings of Mueller, the combination of Gardner with the modulator-related teachings of Mueller is seen as improper.

The Office Action recites that it would be obvious to include a timing error detector as taught in Gardner in the re-sampling circuit of Mueller. This may be true for those teachings of Mueller related to demodulation, but are inapposite for Mueller's teachings related to fractional interpolation at the modulating side of a communication. Regardless, Gardner's timing error detector 106 is seen to have a single input, the strobes Z(m) from the interpolator 120 that are used to correct phase in the VCO 112 (sample timing). Claim 1 recites that the timing error detector sub-circuit has two inputs: one from a symbol rate clock and the other from a strobe. Apart from the NCO/VCO distinction which clearly separates the modulate

from the demodulate side of a communication, this claimed interrelation of components is beyond the combination of Mueller and Gardner.

The Office Action does not appear to address the parallel implementation recited in claim 1, which recites in relevant part:

> an oscillator having...N timing signal outputs for outputting N timing signals in parallel...
> at least one fractional interpolator having parallel inputs coupled to N data inputs in parallel...

This recites a *parallel* implementation of a modulator in which the sample-rate clock is decoupled from the symbol-rate clock (claim 1 recites the oscillator separately from the symbol rate clock). Mueller is not seen to disclose, teach or suggest such a parallel implementation though the office action asserts otherwise in the detailed action at page 3. Such a modification to Mueller is not obvious, and still remains a technical challenge for high-data-rate software-defined radio systems. Even if multiple ones of the claimed "at least one fractional interpolator" were used in a modification to Mueller's teaching so that a series of single-input interpolators were arranged in parallel with one another, the claimed oscillator still has N timing signal outputs for outputting N timing signals in parallel. Mueller has no such parallel implementation.

For example, assume a symbol rate of 180×10^6 symbols per second running in an FPGA with highest clock frequency of 200×10^6 Hz, and a DAC sampling rate of 500×10^6 samples per second. A fractional re-sampling filter for such a system requires a processing capability of 360×10^6 samples per second (2 samples per symbol) at the input and 500×10^6 samples per second at the output. These rates are higher than the FPGA clock. Mueller cannot implement a fractional interpolator for such a system; embodiments of the present invention can because its fractional interpolator (and associated synchronization circuit) operates in parallel. A factor of 3 parallel processing provides processing capability of 600×10^6 samples per second for a design running at the 200×10^6 Hz FPGA clock frequency.

In this case, parallel processing is *not duplicating* the design multiple of times to run multiple independent paths, as might be an obvious modification to Mueller in the manner noted above (multiple single-input interpolators). Figure 2 illustrates a true parallel processing implementation with *one interpolator* on each of the I and Q branches and each having N

parallel inputs ("at least one fractional interpolator having parallel inputs coupled to N data inputs" in claim 1) and *one data-synchronization circuit* ("an oscillator having ...N timing signal outputs for outputting N timing signals in parallel..." coupled to the "timing error detector sub-circuit" in claim 1) constructed to a lower FPGA clock frequency but having a processing capability much greater than that (e.g. 6 x FPGA clock frequency for parallel processing factor of 6). The data can be thought of as coming from one stream in serial then de-multiplexed (serial to parallel operation to achieve the channels shown in Figure 2) then passed through the interpolator. Mathematically this is equivalent to the serial interpolator, but the implementation is unique.

From the discussion of claim 1 above and by the written description, the designator N in claim 1 necessarily denotes a parallel processing factor. Mueller's terminology suggests serial inputting of data into the interpolator, and nowhere describes or illustrates parallel inputs to the interpolator, or parallel clock outputs from the NCO to the interpolator. In fact, the examples presented in Mueller use symbol rates of a few hundred thousand symbols per second and sample rates of tens of million samples per second (e.g. 52×10^6 Hz, see [0038]). Mueller does not indicate that the data inputs are processing in parallel using a device clock slower than the processing capability of the design, in contradistinction to the example above wherein the FPGA runs at 200×10^6 Hz yet the capacity is three times that due to N=3 parallelism.

For at least these reasons, claim 1 is seen to patentably distinguish over the combination of Mueller and Gardner. Mueller does not teach or suggest multiple parallel outputs from the oscillator, and Gardner's error detection circuit neither includes the claimed two inputs nor is coupled to a numerically controlled oscillator.

Claims 13, 17 and 18 are each amended to recite the parallel implementation argued above for claim 1, and are seen to distinguish over Mueller and Gardner for much the same reasons. Claims 16 and 18 are canceled as they would be largely redundant in view of the amendments to their independent claims.

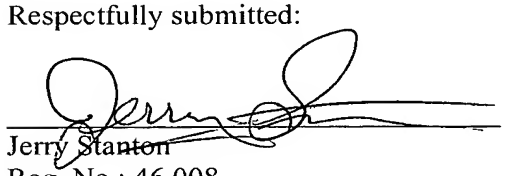
Claim 20 is amended to more clearly recite the parallel implementation detailed above over Mueller. Also as noted above, Herndon is directed to the receive side of a communication,

and fractional interpolation at the receive side differs fundamentally from that at the transmit side due to the different clock synchronizations. Herndon's cited description at [0041] is seen to be simple oversampling. Assuming that Herndon's polyphase filter 600 can be reasonably interpreted as representing a serial to parallel converter that might be implemented in a transmitter (not admitted) and regardless of cyclic independence of sample and output rates, the mere combination of such a serial to parallel converter with Mueller's serial implementation cannot achieve "a numerically controlled oscillator NCO having a plurality of N outputs coupled to respective N inputs of the fractional interpolator for providing N timing signals for respective ones of the interpolated data points" as recited in amended claim 20. Claim 20 is seen to distinguish over the cited combination, which like Gardner and Mueller, is seen to be improper for the modulation side of a communication.

Allowable claim 8 is rewritten to independent form.

All other claims depend from one of those independent claims detailed in the above remarks, and are seen to be patentable at least for that dependency. The Examiner is respectfully requested to review the cited art in view of the above amendments and detailed arguments. The Applicant respectfully requests that the Examiner withdraw the rejections and pass claims 1-15, 17-18, and 20-21 to issue. The undersigned representative welcomes the opportunity to resolve any matters that may remain, formal or otherwise, via teleconference at the Examiner's discretion.

Respectfully submitted:



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